UNIVERSITAT POLITÃLCNICA DE CATALUNYA
BARCELONATECH
Escola PolitÃlcnica Superior d'Enginyeria de Manresa

Final examination

June 11, 2024 | Embedded Systems - iTIC Degree | 120 MINUTES

FAMILY NAME:

GIVEN NAME: ENROLLMENT GROUP:

Question 1 [2 points]. *Fixed point arithmetic*

Considering the notation $\{B, F\}$, with B the number of bits and 2^{-Fa} the value of the LSB (or scaling factor) answer the next questions.

a) Consider the two's-complement binary number '10111' coded with $\{5, 3\}$. Mark the true answer/answers.

- ◯ The range of coded numbers is $\{-2, ..., 1.875\}$
- ◯ The coded value is 2.875
- ◯ The coded value is -1.125
- ◯ Numbers are coded at intervals $\Delta = 0.125$
- ◯ None of the others answers is true

b) Decide the best notation $\{B, F\}$ to code even numbers from -10 to 10. Once decide, code -10 and 10.

Question 2 [3 points]. *ADC*

Regarding the 10-bit analog-to-digital converter (ADC) of the ATmega328P AVR microcontroller answer the next questions considering that we have selected $V_{ref} = 5\,\text{V}$ as the ADC reference voltage.

a) Compute the value of the three MSB given by the ADC, x_{ADC}, if the voltage at the input is $v_{in} = 0.623\,\text{V}$. Mark the true answer/answers.

- ◯ $x_{ADC} = 0$
- ◯ $x_{ADC} = 1$
- ◯ $x_{ADC} = 2$
- ◯ $x_{ADC} = 3$
- ◯ None of the others answers is true

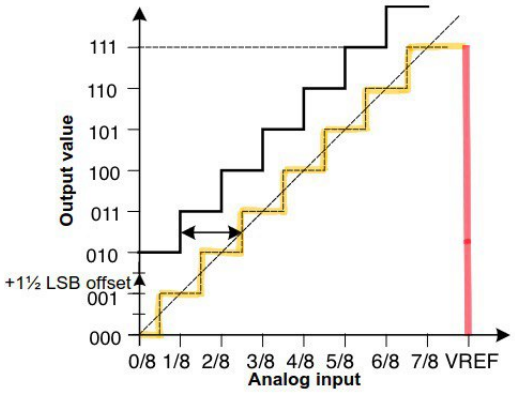
To help you answer this question, here is an excerpt from the ATmega328P datasheet

For single ended conversion, the result is:

$$\text{ADC} = \frac{V_{IN} \times 1024}{V_{REF}}$$

where V_{IN} is the voltage on the selected input pin and V_{REF} the selected voltage reference (see Table 23-3 on page 217 and Table 23-4 on page 218). 0x000 represents analog ground, and 0x3FF represents the selected reference voltage minus one LSB.

and of an ADC application note with an example considering just 3 bits.



b) Justify the previous answer

c) Consider the following types of ADC: Successive Approximation (SAR), Delta-sigma, Dual Slope, Pipelined and Flash. Mark the true answer/answers.

- ◯ SAR has the lowest speed
- ◯ Delta-Sigma is used in voltmeters
- ◯ Dual-slope offers a good balance of speed and resolution
- ◯ Pipelined has the highest speed
- ◯ Flash has the highest resolution
- ◯ None of the others answers is true

d) Explain as much as you know about one of these ADCs.

Question 3 [2 points]. *VHDL: sending data without the help of a clk*

Next you have a `VHDL` code of the *layer 3* of the FPGA course project written by one of the lab groups during this semester. Signal `dat_out` should be read by an ATmega328P AVR microcontroller when `en_out` changes from '0' to '1'.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity layer3 is
  port (clk, clk_en_in: in std_logic;
        dat_in: in std_logic_vector(4 downto 0);
        dat_out: out std_logic_vector(3 downto 0);
        en_out: out std_logic);
end;

architecture rtl of layer3 is
  signal state: std_logic:='0'; --'0' waits for silence, '1' waits for tone
begin
  process(clk)
  begin
    if rising_edge(clk)then
      if clk_en_in = '1' then
        case state is
          when '0' =>
            en_out <= '1';
            if dat_in = "10000" then state <= '1';--silence
            end if;
          when '1' =>
            en_out <= '0';
            if (dat_in /= "10000") and (dat_in /= "10001") then --tone
              dat_out <= dat_in(3 downto 0);
              state <= '0';
            end if;
        end case;
      end if;
    end if;
  end process;
end;
```

a) Draw the actual digital waveform of (`clk`, `clk_en_in`, `state`, `dat_in`, `dat_out` and `en_out`). Consider that there is one `clk_en_in` for every three `clk`, and that `dat_in` alternates between a silence and a tone.

b) Discuss if `en_out` changes at the right moment from '0' to '1'. If not, modify the code (you can erase or add code next to the printed code).

Question 4 [3 points]. *VHDL: a FSM implementation*

Consider again the previous code.

a) Write a *valid* FSM with the *style* that uses three *process*.

b) Discuss the reduction in the number of registers achieved by this implementation.

c) Draw the digital waveform of the relevant signals.