Digital Systems - TestBench

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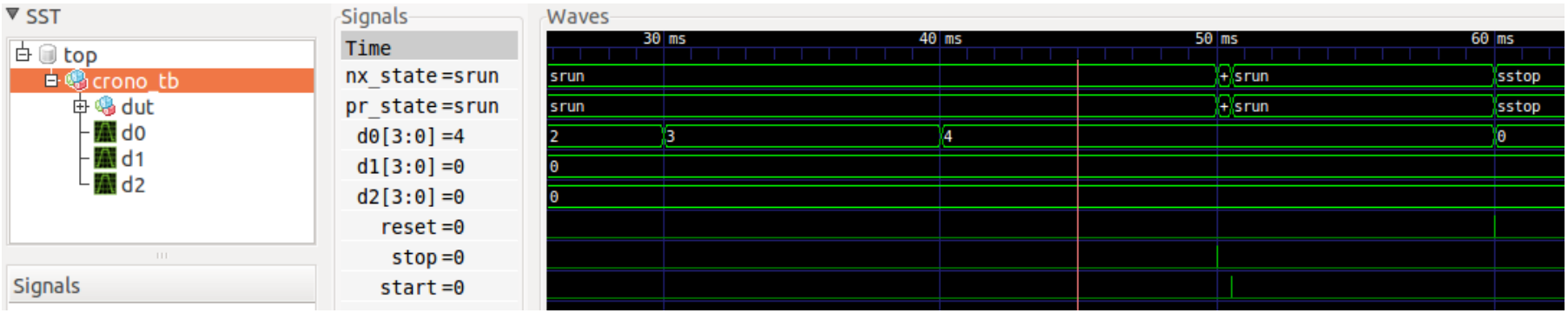
Waveform formats

- The `vcd` format can only handle basic signal types: `bit` `bit_vector` `std_ulogic` `std_logic` `std_ulogic_vector` `std_logic_vector` and integers
- This is a shortcoming when simulating state machines, but this format is quite standard.
- The `ghw` format allows to dump any kind of VHDL signal
- `$ ghdl -a crono.vhd`
- `$ ghdl -a crono_tb.vhd`
- `$ ghdl -e crono_tb`
- `$ ghdl -r crono_tb --wave=crono_tb.ghw`
- `$ gtkwave crono_tb.ghw &`

ghw simulation display

- Example: a state machine with different internal states



- Note that the left pane shows the hierarchy of the testbench
  - Signals defined in the testbench (`reset`, `stop`, `start`)
  - Signals generated by the dut (`d0`, `d1`, `d2`)
  - Internal signals of the dut (`nx_state`, `pr_state`)
- To insert a signal, navigate to its position in the hierarchy and click "insert"