Microelectronics
Exercises of Topic 2

ICT Systems Engineering
EPSEM - UPC

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Autumn 2018

2 Fabrication Technology

EXERCISE 2.1 Describe the following processing steps in modern semiconductor device fabrication:

- Physical vapor deposition (PVD)
- Chemical vapor deposition (CVD)
- Oxidation (dry and wet)
- Photolithography
- Etching (dry and wet)
- Ion implantation
- Solid-state diffusion
- Metallization

EXERCISE 2.2 Define the following concepts and acronyms related to the field of microelectronics, providing application examples, images and any other information deemed relevant to their description:

- EDA Software
- DRC
- VLSI, ULSI, 3D-IC
- Full-Custom Layout Design
- Semi-Custom / Standard Cell Layout Design

- CPLD, FPGA
- Mixed-signal IC
- Monolithic integrated circuit
- Hybrid integrated circuit
- General-purpose integrated circuit
- ASIC
- ASSP
- SiP
- SoC

Exercise 2.3 Describe de following types of integrated-circuit packaging and look for some illustrative images. Note that many of the packaging configurations offer plastic and ceramic variants.

Through-hole (TH) packaging:

- Single-In-line (SIP)
- Dual-In-line (DIP)
- Quad-In-line (QIP)
- Zig-zag-In-line (ZIP)
- Pin-Grid-Array (PGA)

Surface-mount (SM) packaging:

- Small Outline (SO, SOIC)
- Leaded Chip Carrier (LCC)
- Flat Pack (FP)
- Quad Flat Pack (QFP)
- Ball Grid Array (BGA)