Practice 5. Digital circuit synthesis

From VHDL code description to physical CMOS implementation

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The aim of this practice is to present the design process of digital circuits using standard cells, from the VHDL language description to the layout design ready to be manufactured.

1 Qflow digital synthesis

A digital synthesis flow is a set of tools and methods used to turn a circuit design written in a high-level behavioral language like Verilog or VHDL into a physical circuit, which can either be configuration code for an FPGA target like a Xilinx or Altera chip, or a layout in a specific fabrication process technology, that would become part of a fabricated circuit chip.

Qflow is an open-source complete tool chain (`http://opencircuitdesign.com/qflow`) for synthesizing digital circuits starting from Verilog source and ending in physical layout for a specific target fabrication process.

Qflow 1.1 involves four main steps, as shown in Figure 1, namely: Synthesis, placement, routing and final layout generation and display. Each one of these steps will be described in more detail during the practice session and will be achieved with the aid of the following tools:

- **Yosys**: Verilog parser/synthesis;
- **Graywolf**: Cell and pin placement;
- **Qrouter**: Detail router;
- **Magic**: Final layout generator/viewer.

To install this software, please follow the instructions available at `http://opencircuitdesign.com/qflow`. Starting from Ubuntu 15.04, some of these packages may be found at the Ubuntu repositories. You also have to install Qflow itself:

- **Qflow**: Complete tool chain.

As Qflow accepts by default description files in Verilog language, additional VHDL-to-Verilog conversion software will be used (`http://doolittle.icarus.com/~larry/vhd2vl/`, download `vhd2vl-2.5.tar.gz` file or later):

- **Vhd2vl**: VHDL to Verilog converter.

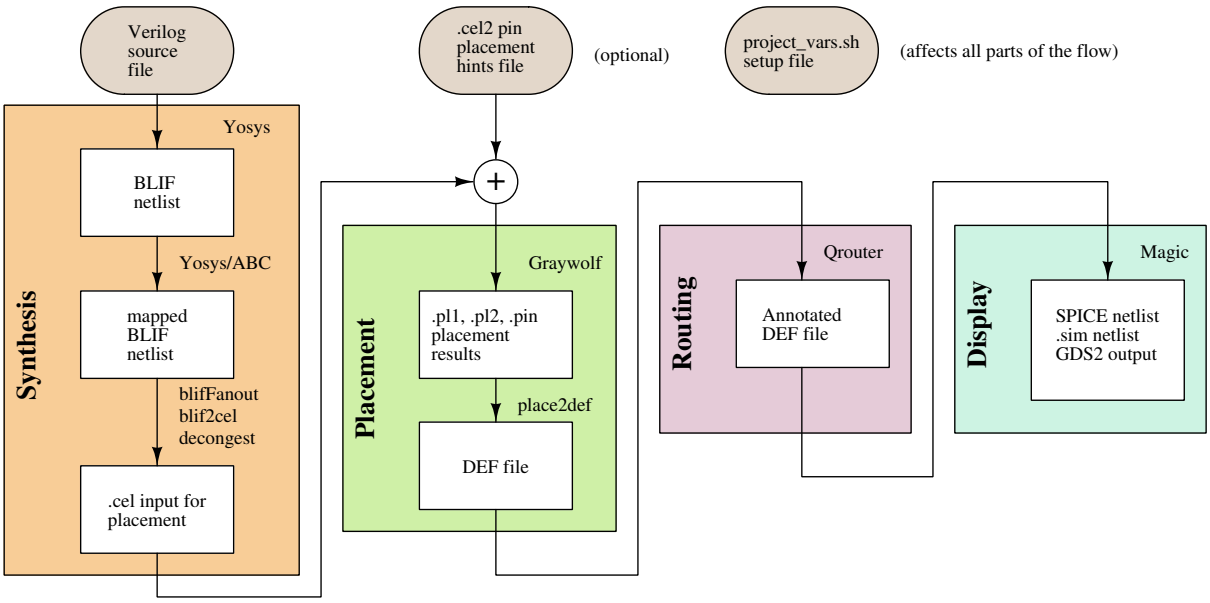

Figure 1

By default, Qflow uses the open-source 0.35 µm standard cell set provided by Oklahoma State University (OSU). The standard cells can be downloaded from http://opencircuitdesign.com/qflow/example/osu035_stdcells.gds2.

Additional open-source standard cells for other technologies provided by OSU can be downloaded from https://vlsiarch.ecen.okstate.edu/flows/MOSIS_SCMOS.

2 Implementation of the flow on specific examples

Task 1. The goal in this first task is to follow the entire flow to implement a simple logic function. Please make the next steps:

a) Write a VHDL file describing a simple logic function. You may consider describing the AND function,

$$F = A \cdot B$$

b) Convert the VHDL file to a Verilog file using vhd2vl.

c) Execute qflow in order to implement the synthesis, placement and routing operations.

d) Execute the corresponding Magic commands, as explained during the practice session, to create the final layout.

e) Display the layout and try to identify the different blocs generated by the flow.

Task 2. Repeat the whole process starting now from the more complex Verilog file *map9v3.v* provided as example by the Qflow web site.