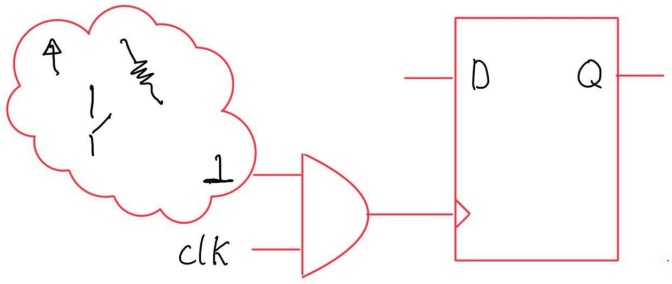
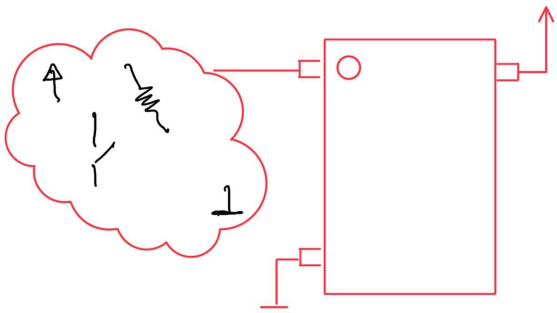
Introduction to Digital Systems
Final examination. January 20, 2022

Time limit: 2.5 hours.
Exam results will be released on January 30, 2022

1. (3 points) We want to stop the clock that arrives to a flip-flop when a switch is closed (i.e. short-circuited). Use a *pull-up* or *pull-down* resistor based design to achieve this behavior completing the following circuit.



2. (3 points) We want the input number 1 of the IC 74HCT00 to be at logic zero, except when a *normally* open switch is pushed (i.e. short-circuited). Use a *pull-up* or *pull-down* resistor based design to achieve this behavior completing the following circuit.



3. (4 points) During this semester we have used three types of special counters to change from one state to another in the particular FSMs in which the future state only depends on the current state: (straight) ring counters, Johnson counters and LFSRs. The advantage of these counters is that, in addition to some flip-flops, they need none or few gates to be implemented.

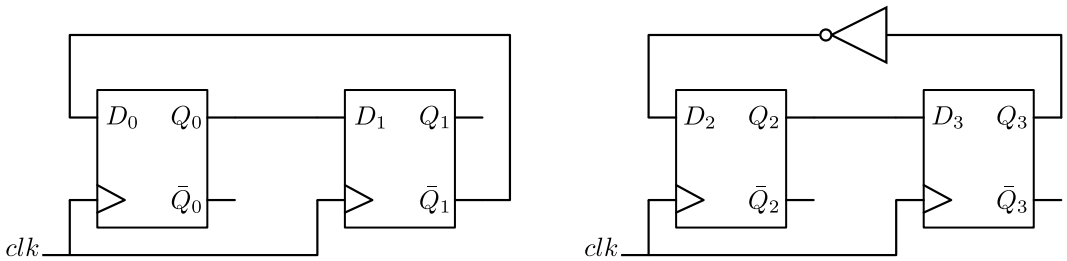
   We have also used custom counters in which the number of gates needed to be implemented changes with the number of values (states) that they take and which order they follow.

   a) (2 points) Discuss the advantages and disadvantages of these 4 types of counter and choose a target FSM for each one.

   b) (1 point) Which counter/counters will you choose to implement a FSM with 7 sequential states? Your goal is to minimize the hardware that has to be used.

   c) (1 point) Which counter/counters will you choose to implement a FSM with 4 sequential states considering that in each state a single output (different for each state) is activated? Your goal is to minimize the hardware that has to be used.

4. (6 points) The two following circuits are slightly different implementations of the so-called Johnson counter.



   a) First, focus on the circuit on the left. Draw the waveform of the relevant signals after *resetting* both flip-flops. Consider ideal flip-flops, i.e. the propagation delay is zero.

   b) Repeat the previous question considering that the flip-flop propagation delay, t_p, is 13 ns. Determine the maximum frequency of the signal *clk* when the *setup* time, t_s, is 7 ns and the *hold* time, t_h, is 1 ns.

   c) Now, focus on the circuit on the right and repeat the previous question, considering that the propagation delay of the NOT gate, t_{NOT}, is 5 ns.

5. (4 points) Consider a 1kB memory, i.e 1024x8bits, with an address bus $\mathbf{A}_0$, a bidirectional data bus $\mathbf{D}_0$, a chip select input $\overline{CS}_0$, and a read/write input $R\backslash\overline{W}_0$.

   a) (0.5 points) Which is the size of the address bus $\mathbf{A}_0$ and the bidirectional data bus $\mathbf{D}_0$?

   b) (2 points) Design a 1024x16bits memory, with signals $\mathbf{A}$, $\mathbf{D}$, $\overline{CS}$ and $R\backslash\overline{W}$. To do this use two 1024x8bits memories, the first with signals $\mathbf{A}_0$, $\mathbf{D}_0$, $\overline{CS}_0$ and $R\backslash\overline{W}_0$, and the second with signals $\mathbf{A}_1$, $\mathbf{D}_1$, $\overline{CS}_1$ and $R\backslash\overline{W}_1$.

   c) (1.5 points) Design a 2048x8bits memory using two 1024x8bits memories and the same signal notation used before.

6. (10 points) During the last year, the so-called self-consumption photovoltaic installations are growing in number. To take advantage of these installations, the owner has to self-consume the energy that is produced **during each hour**.

   Ideally, and oversimplifying the problem, **the energy consumed $E_c(t)$ and the energy produced $E_p(t)$ are considered zero at the beginning of each hour, when $t = 0$, and should be equal at the end of each hour, when $t = 1$ h.**

   To achieve this goal, we could turn ON a load (i.e. a heater) when $E(t) = E_p(t) - E_c(t) > 0$, and turn it OFF when $E(t) = E_p(t) - E_c(t) \leq 0$. The inconvenient with this implementation is that the device that controls the load is switching a lot and, as a consequence, its expected lifetime is shortened.

   The classical solution to this problem uses *hysteresis*. In this implementation, the load is turned ON when $E(t) > E_{ON}$ and it is turned OFF when $E(t) \leq -E_{OFF}$. E_{ON} and E_{OFF} can take any positive value. One of them can also be zero, but if both of them are zero, then there is no hysteresis and we are in the previous implementation.

Consider the following useful information in order to design a FSM that controls the load as a function of $E(t)$:

- E_{ON} and E_{OFF} are parameters and we should not worry about their values.
- $E(t)$ is externally computed and we should not worry about how it is made. Instead, we should (synchronously) reset its value at the beginning of each hour with the output O_1 (high active).
- When $E(t) > E_{ON}$, $I_1 = 1$; otherwise, $I_1 = 0$.
- When $E(t) \leq -E_{OFF}$, $I_2 = 1$; otherwise, $I_2 = 0$.
- The time is externally computed modulo 1 hour. When an hour starts again, $I_3 = 1$ during one clk; otherwise, $I_3 = 0$.
- Consider the following states:
  - INI at which we should go at the beginning of each hour. In this state we reset $E(t)$ and the load is turned OFF.
  - OFF at which we should go/stay after the INI state and when the load must be turned OFF.
  - ON at which we should go/stay when the load must be turned ON.
- The load is turned ON when $L = 1$ and OFF when $L = 0$.

To avoid any misunderstanding: I_1, I_2 and I_3 are inputs of the FSM; O_1 and L are outputs of the FSM.

a) (1 point) How many flip-flops will you use to code the states? Specify the coding of each state with each Q_n. Draw a schematic design that consider the flip-flops, the inputs, the outputs, one combinational block to compute the next state, and another one to compute the outputs.

b) (2 points) Draw a state diagram that includes inputs, outputs and coding of each state.

c) (2 points) Write the truth table of the combinational block that determines the following state, i.e. each D_n. I suggest the following order on the left side of the truth table: I_3 followed by each Q_n, and finally I_2 and I_1. You can use x notation on the left side and don't forget the *don't care* values on the right side.

d) (4 points) Determine the logical function of each output of the previous combinational block. Remember that $f(I_3, Q_n, ...)$ can be computed as $\overline{I_3} \times f(Q_n, ...)|_{I_3=0} + I_3 \times f(Q_n, ...)|_{I_3=1}$. This is useful when you have more that 4 inputs and still want to use the Karnaugh map.

e) (1 point) Write the truth table of the combinational block that determines the outputs and determine the logical function for each output.