

Systems Engineering

Printed Circuit Boards

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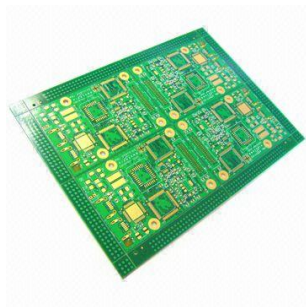
Source: A significant part is from Tim Williams' *The Circuit Designer's Companion*

Introduction

- ▶ Every electronic circuit is built on a PCB
 - ▶ Electrical connections
 - ▶ Mechanical mounting
- ▶ Laminated copper foils
- ▶ Insulating dielectric substrate

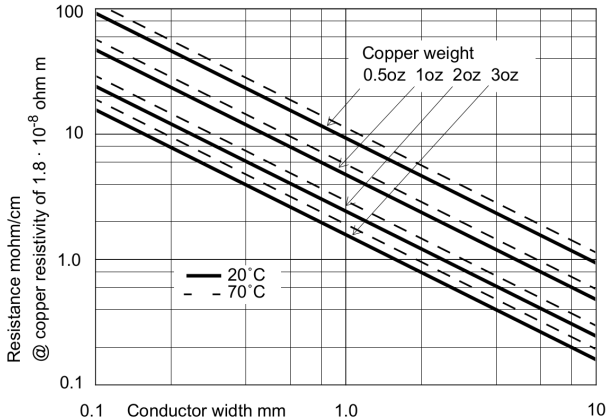
Attention

- ▶ PCB design is a nontrivial task
- ▶ Bad design may compromise functionality



Materials used: Conductor

- ▶ Conductor: copper foil.
- ▶ Bonded to substrate under heat and pressure
- ▶ Standard thickness: $35\mu\text{m}$ (1 oz/sq foot)
- ▶ Other thicknesses: $70\mu\text{m}$ (2 oz/sq foot)



Materials used: Substrates

Usual

- ▶ Epoxy-Glass (FR4)
- ▶ Woven fiberglass + epoxy resin
- ▶ Rated to 130 °

Low-cost

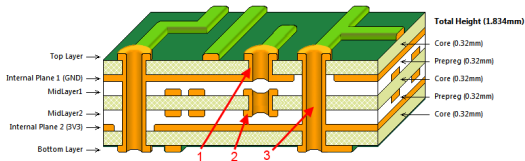
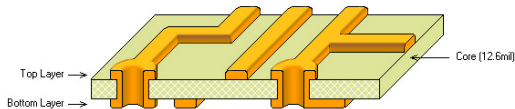
- ▶ Phenolic Paper (FR2)
- ▶ Cheap
 - ▶ Low-end consumer electronics
 - ▶ Single-side boards

Special

- ▶ PTFE (Teflon) (expensive, low dielectric loss, RF, microwaves)
- ▶ CEM3
- ▶ Alumina (Ceramic, very expensive, good thermal conductivity)

Types of Boards

- ▶ Single-sided
- ▶ Double-sided
- ▶ Double-sided, plated-through-holes (PTH)
- ▶ Flexible boards



1. Blind Via
2. Buried Via
3. Through-hole Via

Dimensions and Units

Metric vs Imperial

- ▶ Mixture of metric and imperial units
- ▶ A source of problems!
- ▶ Standard pin spacing 100 mil = 2.54 mm
- ▶ Modern pin spacings 0.5 mm
- ▶ standard SMD resistor 0805 (imperial)=2012 (metric)

PCB shape and dimensions

- ▶ Plan the enclosure first!
- ▶ Design PCB accordingly
- ▶ Standard size: Eurocard (100 × 160 mm)

CAD Packages

- ▶ KiCad 7.0
 - ▶ Open Source
 - ▶ Limited number of libraries
- ▶ Eagle
 - ▶ Free up to certain size
 - ▶ Big community
- ▶ Altium
 - ▶ Expensive
 - ▶ CircuitMaker: free for free projects

Layers

- ▶ Top layer, bottom layer
- ▶ Top soldermask, bottom soldermask
- ▶ Top overlay, bottom overlay
- ▶ Mechanical (Outline)

Data Formats

Artwork

- ▶ Historically separated from drill files
- ▶ Extended Gerber (RS-274X)
- ▶ Gerber “X2” is Gerber with attributes e.g. FileFunction
- ▶ Includes everything in a single file. One file per layer

Drilling

- ▶ Excellon / Drill file format / Gerber format
- ▶ One file for plated, one file for non-plated holes

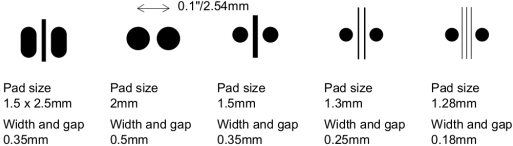
Attention

- ▶ Same units and resolution for everything. No offsets!
- ▶ All layers are viewed from the top! Never mirror anything!
- ▶ Some fabs want an IPC-D-350A netlist file for testing.

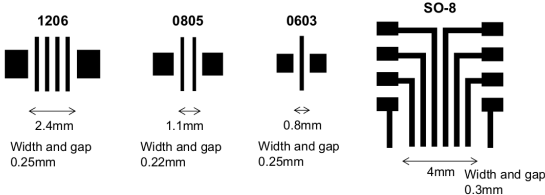
Pads, Vias, ...

- ▶ Pad: components. Round, Oval, Square...
- ▶ Bigger pads for non-PTH holes. Adhesion.
- ▶ Hole: 0.8 mm for through-hole / 1.3 mm pad diameter
- ▶ Hole diameter *after* plating. Manufacturer!
- ▶ Vias connect tracks on different layers. 0.5mm
- ▶ Avoid using multiple hole sizes!

Through-hole (DIL)



Surface mount



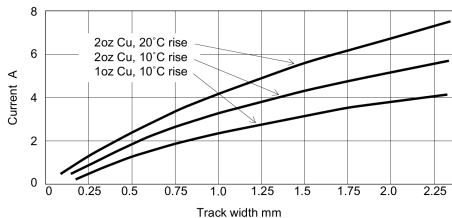
Design rules

Given by manufacturer and process (\$)

Basic Manufacturer

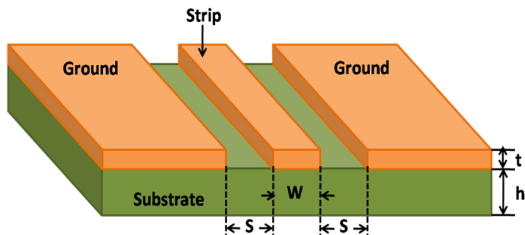
- ▶ Minimum track on copper: 0.2 mm
- ▶ Minimum spaces on copper layers: 0.2 mm
- ▶ Minimum drill hole: 0.6 mm
- ▶ Maximum drill hole: 5.0 mm
- ▶ Minimum annular copper ring around the holes: 0.2 mm

Track Width and Current Capacity



Track Width and Characteristic Impedance

- ▶ FR4 has loose specification on ϵ_r !
- ▶ Transmission Line
- ▶ Microstrip
- ▶ Stripline
- ▶ Coplanar

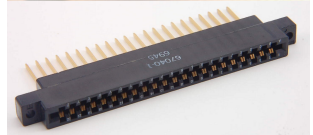
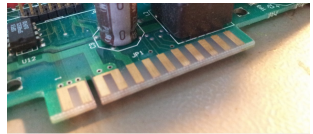
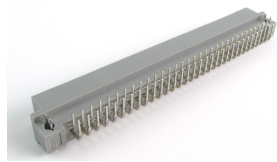


Routing

- ▶ Coupled with placing parts and subparts within package.
- ▶ Short tracks
- ▶ Consider signal returns. Ground inductance!
- ▶ Do not autoroute
- ▶ Ground plane. Power plane. Avoid slots.
- ▶ Thermal relief for planes/polygons
- ▶ Bends at 45 °(or

Connectors

- ▶ Simplest: Wire soldered to pad (PTH)
- ▶ Two-part connectors
- ▶ Beware of force! Screw them before soldering!
- ▶ Edge connectors
- ▶ Screw terminal blocks



Assembly

- ▶ Solder process
 - ▶ Plan for it during PCB design: Package placement
 - ▶ Inspection easier if same orientation in all packages
 - ▶ Component identification. Orientation
- ▶ Reflow oven
- ▶ Cleaning
 - ▶ Remove solder flux. May corrode board. No-clean flux.
- ▶ Testing
 - ▶ Design board for testability