Digital Systems - 7

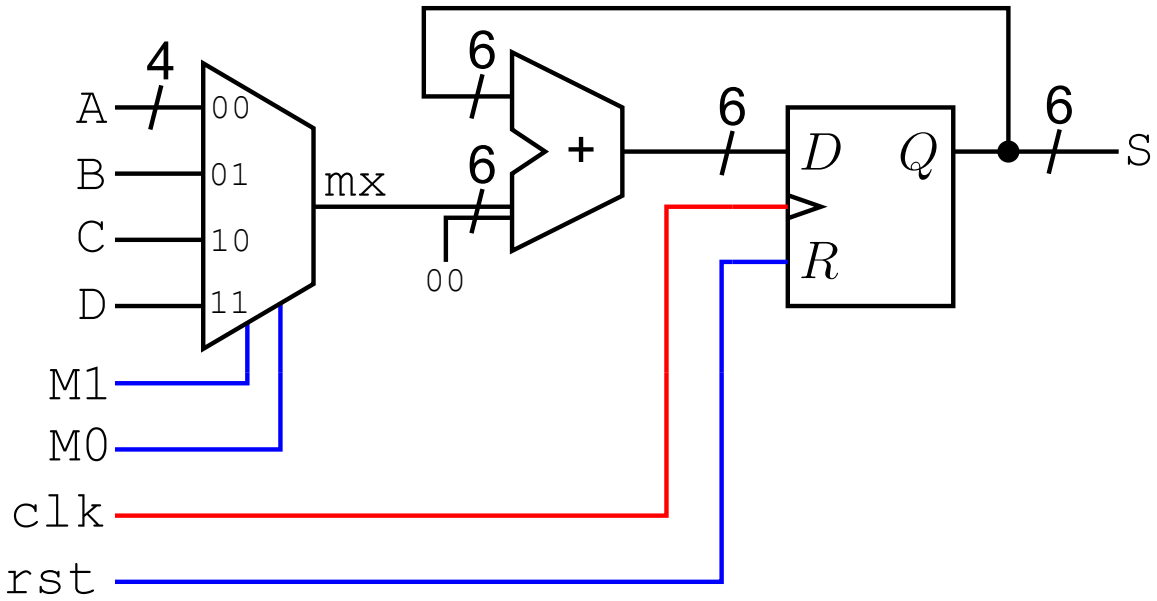
Pere Palà - Alexis López

iTIC http://itic.cat

March 2016

Register Transfer Level Description (1/2)

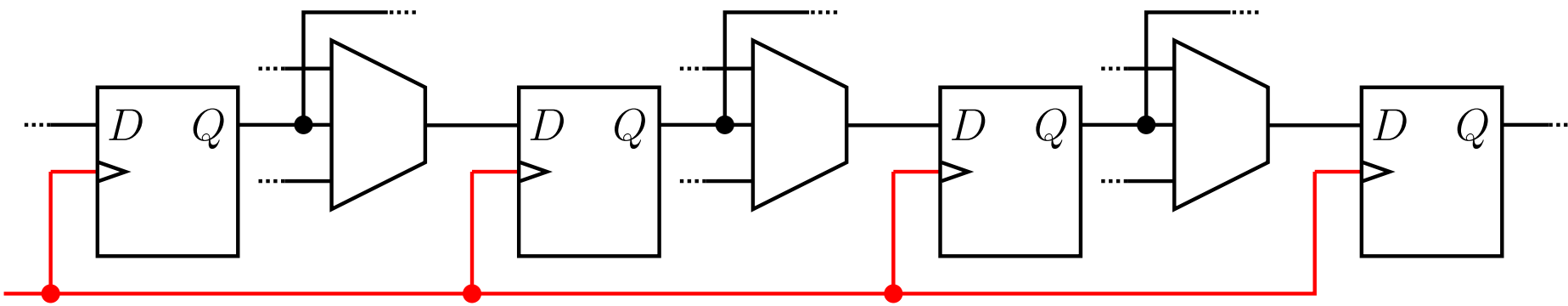
- Our example...



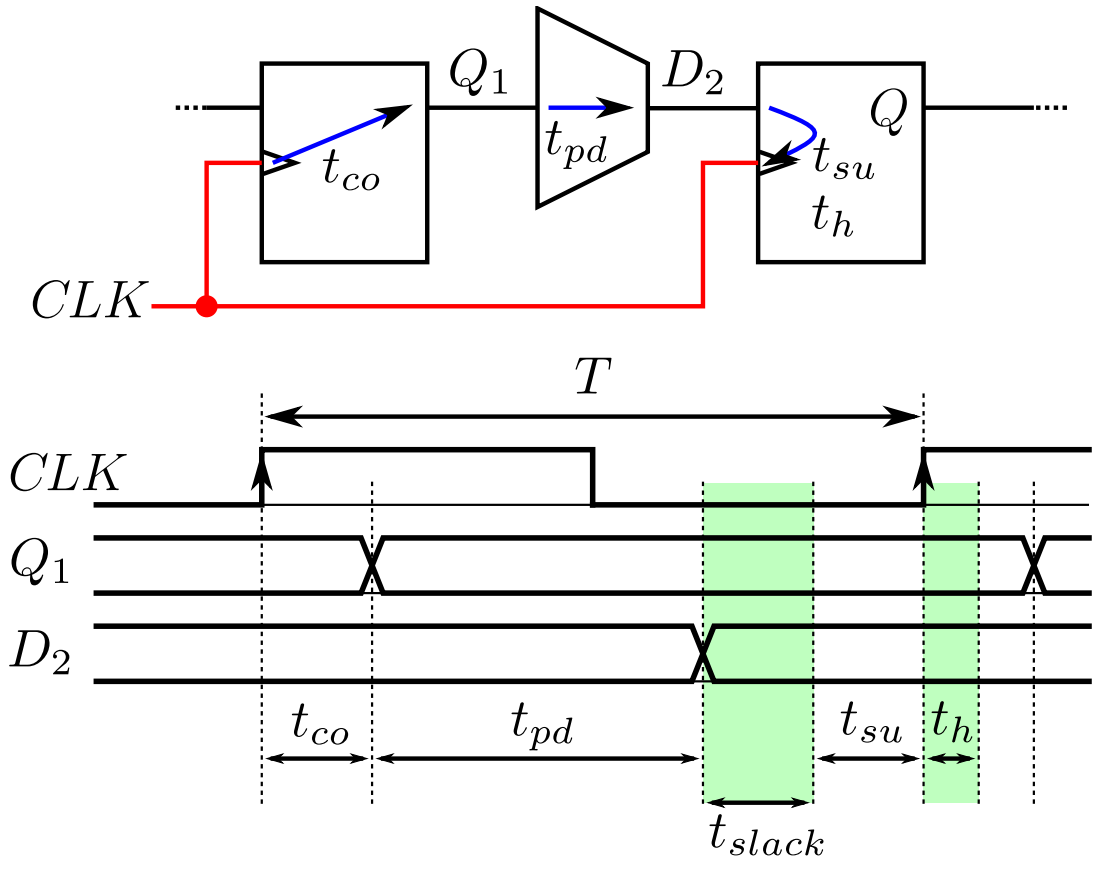
- ... is a specific case of ...

Register Transfer Level Description (2/2)

- General Synchronous System



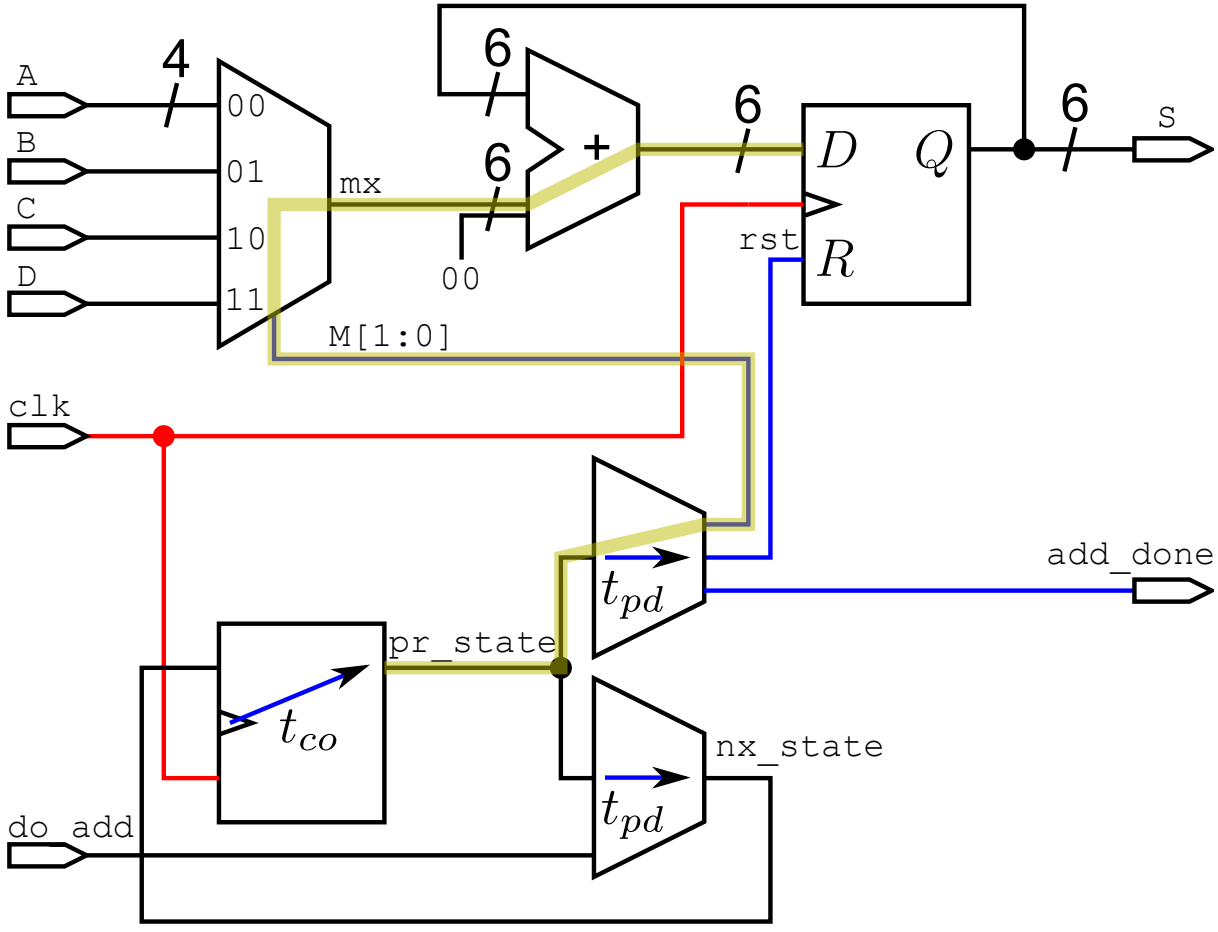
Synchronous Timing



- t_{co}, t_{pd} and t_{su} ns are device-dependent.

Critical Path

- The control path adds (a significant amount of) delay.
- Critical path: Combinational path between register with the longest delay.



Timing Constraints

Views

- First interpretation: $T > t_{co} + t_{pd} + t_{su}$
- Sets a limit on the maximum clock frequency.

- Second interpretation: $t_{pd} < T - t_{co} - t_{su}$
- Sets a limit on the maximum combinational delay.

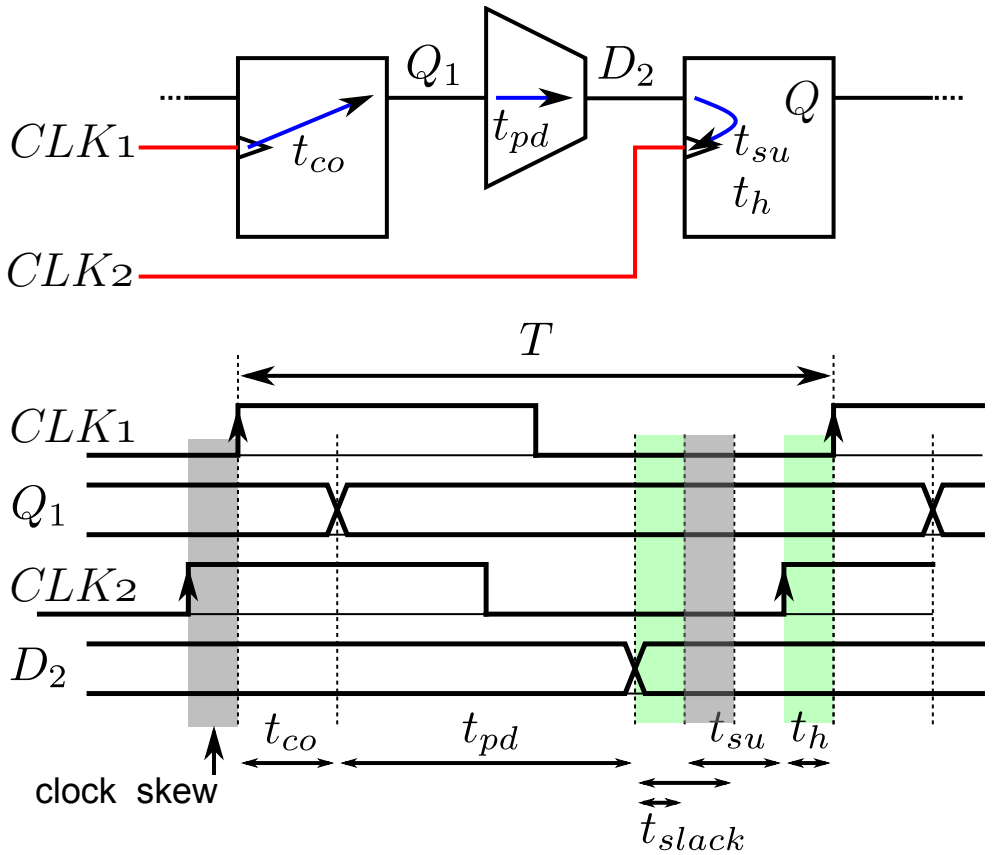
Solution

- Choose a better implementation technology.
- Trade area (complexity) for speed.
- Pipelining: Breaking the longest combinational delay in parts, using intermediate registers. This adds some clocks of latency.

Clock Skew (1/2)

Problem

- Clock net is not able to do deliver edges which are exactly synchronous.
  - At the board level.
  - And even inside the FPGA.



Clock Skew (2/2)

Solution

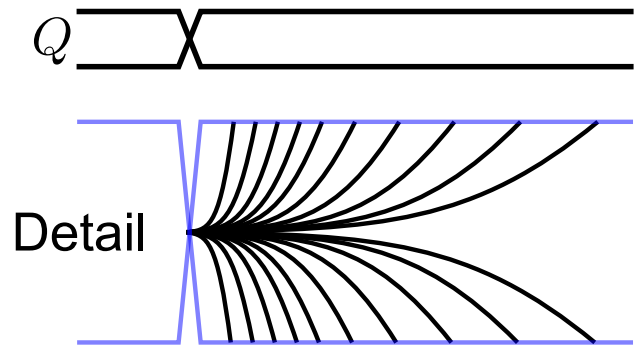
- Reduce clock to accommodate skew.
- Suitable clock distribution network.
- Line length equalization.
- Inserting delays in clock network.

Outside Connections

- Additional delays at connections
  - Pin delays.
  - Wiring delays.
- Exactly the same timing rules.
- Inputs and outputs may be registered to avoid extra delay in the critical path

Asynchronous Inputs

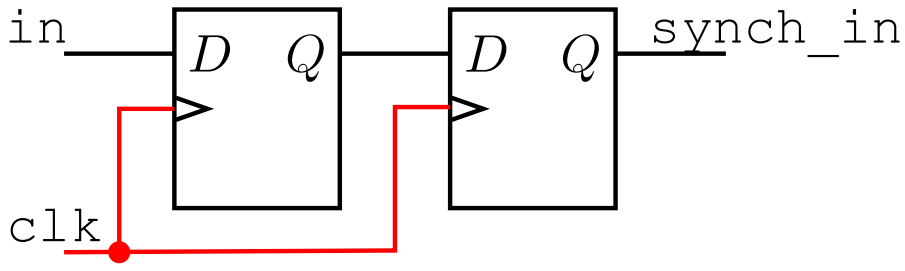
- External inputs may change at any time.
  - May violate setup or hold time constraints.
  - Unavoidable!
- The output of the flip-flop has an exponential evolution with time:



- Destination registers may interpret the signal differently as they are not clearly '1' or '0': System failure.
- Allow sufficient time for the flip-flop to stabilize.

Synchronizer

Two-stage synchronizer



- Normal case: Input is delayed by one extra clock period.
- First flip-flop has one clock period to stabilize.
- Only affects the second flip-flop: No incoherent signals in the system.

Slow Inputs and Bouncing

Hardware Solutions

- S-R flip-flop with SPDT switch.
- RC filtering.
- Schmitt Trigger.

- Pros: No digital resources spent.
- Cons: Components, connections, reliability. Fixed solution.

Software Solutions

- Take successive samples of input signal.
- Look for n ($n > 1$) successive samples which are different that the current state. Signal the change.

- Pros: No additional components. Only FPGA. Configurable.
- Cons: Consumes digital resources.