Microelectronics
Exercises of Topic 3

ICT Systems Engineering
EPSEM - UPC

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3 Active and passive devices in integrated circuits

EXERCISE 3.1 The diagram in Figure 1 shows the internal structure of an N-channel enhancement MOS transistor.

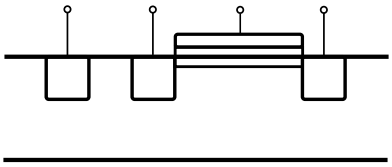

Figure 1

a) Complete the diagram describing each of the materials that constitute the transistor and the function performed.

b) Draw in detail how the diagram above changes in the different modes of operation of the transistor and explain qualitatively the behavior of the device in each case.

EXERCISE 3.2 Repeat the previous exercise for the following types of transistor:

a) P-channel enhancement MOST;

b) N-channel depletion MOST;

c) P-channel depletion MOST.

EXERCISE 3.3 We want to design an N-channel MOS transistor to be used as a switch. In particular, we need a conduction resistance $R_{DSon} = 1\ \Omega$ when $V_{GS} = 5$ V. Knowing that $K' = 20\ \mu\text{A/V}^2$ and $V_T = 1$ V, determine the ratio W/L (supose that conduction takes place with $V_{DS} \simeq 0$).

Exercise 3.4 In the design of an electronic circuit to be integrated in 2-µm CMOS technology, we want to use an N-channel MOS transistor to implement a linear resistor of 1.1 kΩ connected to the reference node (ground) through one of its terminals. To this end:

a) Based on the equations of the MOS transistor, indicate the requirements that V_{GS} and V_{DS} must accomplish so that the device behaves as a linear resistor (i.e., so that it exhibits I_D proportional to V_{DS}).

b) Knowing that the supply voltage is $V_{DD} = 5$ V, $K' = 20$ µA/V^2 and $V_T = 0.5$ V, find the proper dimensions of the transistor.

c) Draw the resulting circuit schematic clearly indicating the terminals of the desired resistance.

d) Specify the range of voltages that can be applied to this resistance so that the transistor provides the expected behavior.

Exercise 3.5 Questions C8.1, C8.3, C8.4 and C8.11 (page 321) in Prat et al. [1].

Exercise 3.6 (NMOS inverter) Guided problem 6.3 (page 335) in Prat and Calderer [2].

Exercise 3.7 (CMOS inverter) Guided problem 6.4 (page 336) in Prat and Calderer [2].

Exercise 3.8 (CMOS inverter) Exercise 1.7 (page 1.15) in Castañer et al. [3]. The inversion voltage V_{INV} is defined in the same page of the exercise statement.

Exercise 3.9 For the circuit in Figure 2 find the operating point of the transistor, i.e., the variables v_{GS}, v_{DS} and i_D. Verify the results by means of simulation.

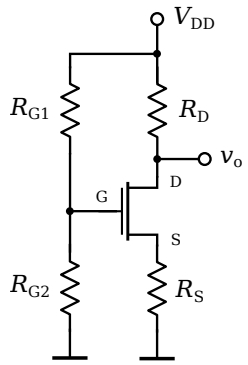

Figure 2

$V_{DD} = 20$ V, $R_{G1} = 100$ kΩ, $R_{G2} = 100$ kΩ, $R_S = 10$ kΩ, $R_D = 10$ kΩ,
$K' = 20$ µA/V^2, $W/L = 10$, $V_T = 1$ V.

EXERCISE 3.10 We want to design a logic inverter to be fabricated in 2-µm NMOS technology, according to the schematic in Figure 3, where $V_{DD} = 5$ V.

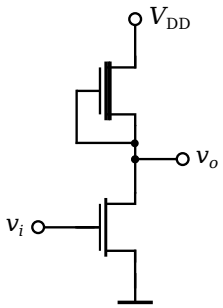

Figure 3

In particular it is required that when the output is at the low level the voltage does not exceed the value $v_o = 0.5$ V. The dimensions of the enhancement NMOSFET (transistor below) are $W = 3$ µm, $L = 2$ µm, with a threshold voltage $V_T = 0.5$ V. The depletion NMOSFET (transistor above) has a theshold voltage $V_T = -0.5$ V. In both cases we have $K' = 20$ µA/V^2.

a) For each of the logical states available at the input ($v_i = 0$ V and $v_i = 5$ V), indicate in a reasoned manner the mode in which the transistors operate.

b) Determine the minimum dimensions of the depletion NMOSFET.

EXERCISE 3.11 Suppose that you have to design a CMOS voltage divider that provides an output voltage $v_o = 0.75$ V from a power supply voltage $V_{DD} = 1.5$ V, as shown in the schematic in Figure 4.

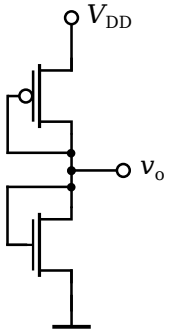

Figure 4

The technology used is 180 nm with the following parameters: minimum device width $W =$ 240 nm, $K'_P = 10$ µA/V^2, $K'_N = 20$ µA/V^2, $V_{TP} = -0.5$ V and $V_{TN} = 0.3$ V.

a) Indicate de mode of operation of the transistors.

b) Determine the corresponding device dimensions, knowing that the current consumed by the divider must not exceed 10 µA.

EXERCISE 3.12 In this exercise you must determine the best strategy to implement resistors in an integrated circuit using 2-µm CMOS technology. The following table shows different techniques available with their characteristic parameters (sheet resistance R_s in the case of layers) and their minimum dimensions:

Layer / Device	Parameter	Minimum size
- N+ diffusion	$R_s = 35\ \Omega$/square	$W = L = 3\ \mu$m
- Polysilicon	$R_s = 65\ \Omega$/square	$W = L = 2\ \mu$m
- N well	$R_s = 2\ \text{k}\Omega$/square	$W = L = 10\ \mu$m
- Enhancement NMOS transistor operated as a saturated load	$K' = 70,28 \times 10^{-6}$ A/V^2 $V_T = 0.7$ V	Channel: $W = 3\ \mu$m, $L = 2\ \mu$m

Knowing that the design requires to implement the following resistance values,

- 100 Ω
- 10 kΩ
- 1 MΩ

find the best option for each case. Set as the primary objective to occupy as little area as possible. In the case of the saturated load, assume that it supports a voltage of 2.5 V.

References

[1] Prat, Ll.; Bragós, R.; Chávez, J. A.; Fernández, M.; Jiménez, V.; Madrenas, J.; Navarro, E.; Salazar, J. *Circuitos y dispositivos electrónicos. Fundamentos de electrónica*. 6a ed. Barcelona, Edicions UPC, 1999. ISBN: 84-8301-291-X

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http://upcommons.upc.edu/handle/2099.3/36340

[2] Prat, Ll.; Calderer, J. *Dispositius electrònics i fotònics. Fonaments*. 2a ed. Barcelona, Edicions UPC, 2006. ISBN: 84-8301-855-1.

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[3] Castañer, L.; Jiménez, V.; Bardés, D. *Fundamentos de diseño microelectrónico*. Barcelona, Edicions UPC, 2002. ISBN: 84-8301-613-3.

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